Entegris

Advanced CMP of Silicon Carbide for EVs and Power ICs

White paper

INTRODUCTION

The transition from gas-powered to electric vehicles (EVs) is happening at a faster rate than was predicted a few years ago. Batteries are also operating at higher voltages. Both these trends put pressure on power integrated circuit (IC) manufacturers to produce higher volumes of chips using technologies designed to withstand high-temperature, high-frequency operating environments. Part of the answer lies in transitioning from silicon substrates to silicon carbide (SiC) and gallium nitride (GaN).

The need to cope with higher operating voltages, which are moving from 650 V to 1200 V and above, favors SiC over both silicon and GaN. SiC can tolerate much higher temperatures and improve device electrical performance. In terms of switching efficiency, SiC outperforms silicon by an order of magnitude.

High-performance SiC-based transistors are a relatively new technology, with the automotive industry's first commercial SiC MOSFET introduced in on-board chargers for electric vehicles a decade ago. These devices first premiered in Tesla vehicles but have since expanded to other EVs.

Power IC demand is exploding as multiple major automotive companies race to ramp up EV production and release new models with longer driving range.[1] Market research firm Yole Développement expects the power IC market to triple between 2020 and 2026. The automotive industry is driving the bulk of this increase, Figure 1.

While SiC wafers are more expensive than silicon, costs for SiC-based discrete chips and modules are expected to drop with higher volumes and the transition to larger wafers.

The automotive industry is currently facing a supply shortage for many of the chips required to produce today's vehicles, let alone the volumes that will be required in coming years. This includes power ICs for EVs.

The market conditions provide both a challenge and an opportunity for the semiconductor industry. First, ingot manufacturers must ensure an adequate supply of SiC wafers. That alone, however, is not enough. Beyond sourcing raw materials, the market demands improvements in both throughput and electrical performance.

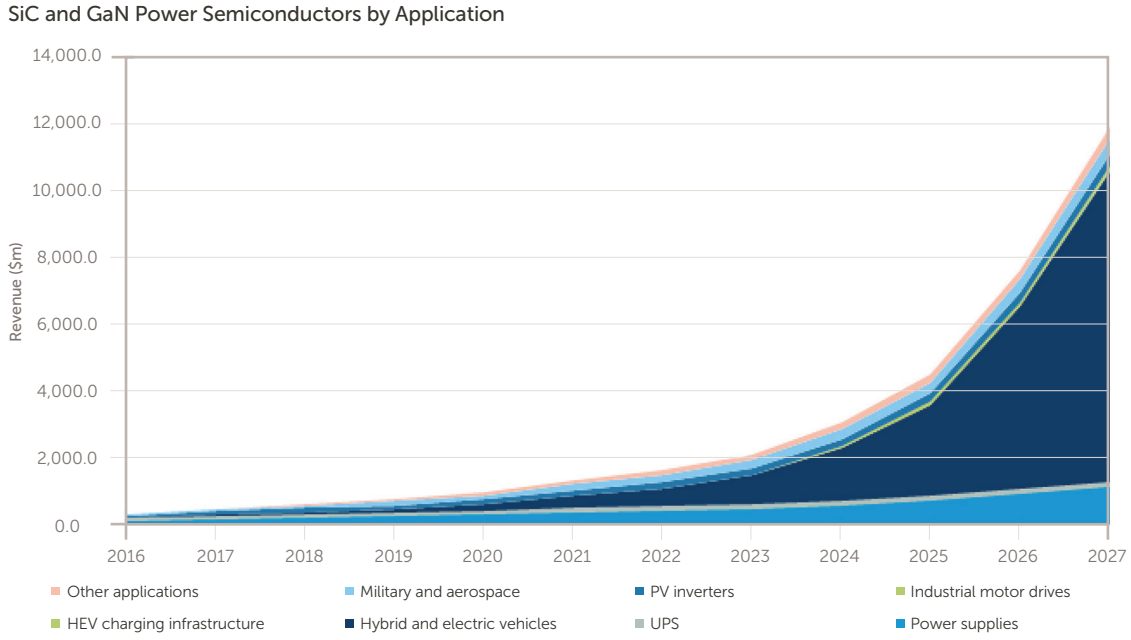

Figure 1. Forecasted market for SiC and GaN power devices. Hybrid and electric vehicles (dark blue) represent the bulk of projected growth. Source: IHS Markit, 2018.

Solutions that improve utilization rates of SiC materials and reduce cost of ownership (COO) will be especially valuable. The first steps in fabricating SiC wafers involve grinding, lapping, and polishing the wafers to create the necessary surface properties before depositing active layers. The slurries used to carry out these steps, therefore, are becoming more critical.

Chemical mechanical planarization (CMP) that is optimized for SiC wafers can support greater throughput and higher yield, thereby mitigating the supply chain challenges and reducing COO. This white paper describes challenges specific to CMP of SiC wafers and proposes solutions to improve SiC slurry performance and meet the needs of power IC manufacturers.

CMP OF SiC WAFERS: CURRENT CHALLENGES

The manufacturing of SiC wafers from SiC boules involves multiple steps:

1. Sawing to cut the wafer from the boules,
2. Grinding with large diamond particles to remove the wire saw marks,
3. Lapping with smaller diamond particles (particle size 2-3 micron) to remove the subsurface damage from the earlier step, and
4. CMP to achieve a smooth finish for subsequent epitaxial deposition.

CMP slurries perform a critical role to ensure wafer quality and subsequent yield. Parameters such as slurry composition, applied force, and pad materials must be adjusted to be compatible with the SiC substrate and achieve the desired surface conditions.

When using CMP to polish SiC wafers, several challenges are limiting performance. SiC is a hard, chemically inert material that is much more difficult to polish than silicon. The CMP process should achieve a scratch-free, smooth surface that is uniform across the wafer, but that result is not guaranteed.

As with all CMP slurries, both the abrasives and the chemical additives affect the polishing results. But because SiC is inert, it is resistant to the chemicals that are effective on silica surfaces. The hardness of SiC – three times that of amorphous silica – means that standard CMP abrasives like silica and alumina result in extremely low material removal rates and, therefore, long polishing times. Fabs cannot afford to spend dozens of hours polishing one batch of wafers. Hard particles, such as diamond, remove material faster but cause significant scratches, both at and below the wafer surface.

Fast removal rates are desirable to increase throughput and reduce the COO, but merely increasing the abrasive content to achieve faster material removal is not an optimal solution. Higher abrasive content makes the slurry more expensive. An abrasive content that is too high also results in a nonuniform finish and greater prevalence of scratches that cause defects. Similarly, increasing the pressure also induces undesirable scratches on the wafer.

An ideal solution will achieve high polishing rates by rapidly removing a self-passivating nanoscale layer at the surface of the wafer, Figure 2. The removal rate should be highly pressure sensitive to ensure planarity across the wafer, but such sensitivity puts tighter constraints on process control.

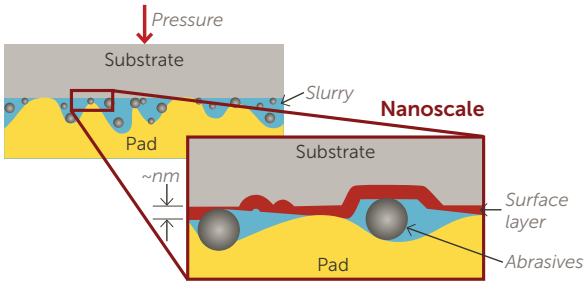

Figure 2. Removal of nanolayer material from wafer surface via CMP.

ADVANCED SOLUTIONS TO IMPROVE SiC CMP

Diamond Lapping

Diamond abrasives are an excellent solution for bulk removal (lapping and grinding) of SiC, where fast removal rate is the top priority. The larger the particle size, the faster the removal rate. Larger particles, however, like those in standard micron-scale diamond lapping slurries, produce relatively rough surfaces and extensive subsurface damage.

Due to variations in diamond particle size distribution, the lapping step may create regions of higher subsurface damage that the final CMP step does not remove.

To reduce the severity of scratches, slurry formulations that incorporate smaller proprietary engineered nanodiamond particles can achieve rapid SiC removal with minimal subsurface damage. This technique improves results for the lapping step on SiC wafers. Removal rates are as high as those achieved with larger diamond particles while creating a much smoother surface with a greatly decreased and more uniform damage profile. Using these engineered nanodiamond particles makes the subsequent CMP step much faster and more predictable.

CMP Polishing

The final CMP polishing step requires a different approach. The challenge of efficient CMP on SiC wafers can now be solved by migrating away from conventional CMP slurry formulations to engineered particles and additives tailored to enhance the surface reaction kinetics of SiC. These unique combinations of chemicals can achieve relatively high removal rates along with improved surface finish. They do so with precise, localized chemical action in a method called reactive CMP, Figure 3.

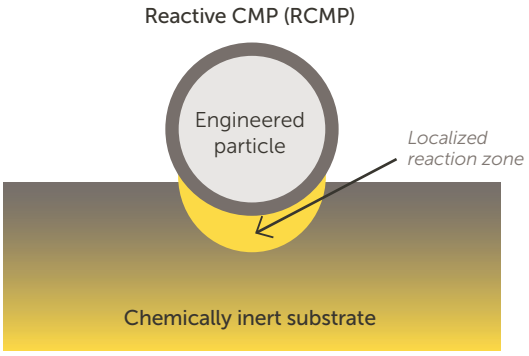

Figure 3. Reactive CMP for final polish on SiC wafers.

As with all CMP processes, the slurry is the most important element but is not the only aspect to consider. A synergistic approach is the best way to ensure high yields.[2] The pad must be compatible with the slurry to achieve the required planarity when polishing SiC wafers. A pad that is too hard, however, increases the prevalence of scratches and particle contamination. When the pad and slurry are optimized to work together, CMP can be performed using lower pressure and yields increase.

Post-CMP cleans must also be formulated to efficiently remove the slurry before moving to the next fabrication step. The cleaning step eliminates chemical contaminants and abrasive particles that, if left on the wafer, would compromise deposition of subsequent layers.

MEETING FUTURE NEEDS

Because of the trend toward higher frequency and higher voltage applications, CMP processes that have worked for the past few years are no longer good enough. Flatness specifications across a wafer are more demanding for 5G operations than they were for 4G. Fine scratches that were previously accepted now create reliability issues.

Wafer sizes are also increasing. The SiC market is moving from 150 mm to 200 mm wafers. This shift, while producing more chips per wafer, also makes it more challenging to achieve a planar, uniform surface across the entire wafer. The batch polishing tools in common use for 100 and 150 mm wafers cannot achieve repeatable results for larger wafers. Fabs are likely to transition to tools that process one wafer at a time, making throughput a greater challenge.

Lapping and polishing must be improved to take advantage of the process efficiencies that larger wafers enable. Higher polish rates are necessary, but faster polishing must not sacrifice surface quality.

As performance demands are increasing, so are cost pressures. The tight SiC supply means that producing more good wafers per ingot is critical. The larger the ingot diameter, the more valuable the wafer. For both these reasons, lower scrap rates are essential.

The combination of lapping with smaller nanodiamond particles and polishing with nontraditional CMP slurry chemistries described above addresses the requirement for smoother, more uniform surfaces. The improved finish of the base layer will allow subsequent patterned layers to achieve lower defect rates and, therefore, higher device yields.

Higher device yield reduces COO, as does shorter CMP time. Consumption of process chemicals is another consideration when addressing COO of the CMP process. Dilutable slurries offer a solution.

Instead of using slurries as delivered, fabs can customize the formulation by diluting concentrated slurries to a level that meets each application's needs. Compared to previous formulations, dilutable slurries are much more efficient. These newer slurry chemistries allow fabs to use lower chemical volumes while achieving fast material removal rates with no loss in CMP performance.

ENABLING PROGRESS FOR EVS AND OTHER APPLICATIONS

While SiC-based power ICs are needed to support the expanding EV market, that is far from the only sector that can benefit from SiC devices. SiC MOSFETs are needed for solar inverters as well as EV inverters and are making their way into applications ranging from industrial power supplies to home appliances.

Penetration of SiC into new applications will rely even more heavily on cost reductions. Fabrication on larger wafers is part of the answer, but it must be done in conjunction with a nonlinear departure from existing CMP methods. Nontraditional CMP chemistries will enable progress by achieving faster material removal while offering smoother SiC surfaces and higher yields.

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References

[1] Phil Covington, *Ford the Latest Automaker to Make Bold EV Commitment*, Triple Pundit, 25 February 2021, https://www.triplepundit.com/story/2021/ford-ev-commitment/719021

[2] *Particles, Processes, and Planning: Synergies to Improve CMP Yield*, Entegris white paper, April 2021.

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